

**FORM PTO - 1449** 

## SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

ATTORNEY DOCKET NO.: ASC-022CPC1

APPLICANT(S): Wu et al.

SERIAL NO.: 10/603,852

FILING DATE: June 25, 2003

GROUP: 2811

## **U.S. PATENT DOCUMENTS** SUB CLASS FILING DATE IF EXAM. DOCUMENT DATE NAME **CLASS** APPROPRIATE . INIT. NUMBER 2002/140031 10/03/2002 Rim A249 A1 2003/003679 A A250 01/02/2003 Doyle et al. 5.013.681 Godbey et al. A251 05/07/1991 A252 5,548,128 08/20/1996 Soref et al. A253 5,607,876 03/04/1997 Biegelsen et al. A254 5,906,951 05/25/1999 Chu et al. A255 6,154,475 Soref et al. 11/28/2000 6,372,593 B1 04/16/2002 Hattori et al. A256 12/03/2002 Hoke et al. 6,489,639 A257 6,521,041 A258 02/18/2003 Wu et al. A259 6,591,321 Arimilli et al. 11/09/1999 07/08/2003 01/13/2000 A260 6,597,016 07/22/2003 Yuki et al. 01/06/2004 Takagi et al. 04/03/2002 6,674,150 A261 06/22/2000 6,689,211 02/10/2004 Wu et al. A262 FOREIGN PATENT DOCUMENTS ENGLISH FILING **ABSTRACT** EXAM. DOCUMENT DATE COUNTRY CLASS SUB LANG (Y/N) INIT. NUMBER CODE **CLASS** DATE ONLY B53 02-098158 04/10/1990 JР 06-196673 07/15/1994 JP Υ B54

EXAMINER Ongla W. Owen	DATE CONSIDERED 10/65/05



**FORM PTO - 1449** 

## SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

ATTORNEY DOCKET NO.: ASC-022CPC1

APPLICANT(S): Wu et al.

SERIAL NO.: 10/603,852

FILING DATE: June 25, 2003

GROUP: 2811

## OTHER ART, JOURNAL ARTICLES, ETC. OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication) EXAM. INIT. Canaperi et al., "Preparation of a relaxed Si-Ge layer on an insulator in fabricating high-speed semiconductor devices with sustained epitaxial films", IBM, USA (2002) (abstract). Decision of Rejection for Japanese Patent Application Serial No. 2000-544004, August 20, 2002, 2 pages. Godbey et al., (1990) "Fabrication of Bond and Etch-Back Silicon Insulator Using a Strained Slo.7GE0.3 Layer as an Etch Stop," Journal of the Electrical Society, Vol. 137, No. 10 (October 1990) pp. 3219-3223. Huang et al., (2001) "Carrier Mobility enhancement in strained Si-on-insulatoir fabricated by wafer bonding", 2001 Symposium on VLSI Technology, Digest of Technical Papers, pp. 57-58 C150 International Search Report for International Application No. PCT/US99/07849, August 16, 1999, 5 pages. C151 International Search Report for International Application No. PCT/US01/46322, January 22, 2003, 4 pages. C152 International Search Report for International Application No. PCT/US03/18007, January 5, 2004, 6 pages Langdo et al., (2002) "Preparation of Novel SiGe-free Strained Si on Insulator Substrates" IEEE International SOI Conference, pages 211-212 (XP002263057) Notice of Grounds of Rejection for Japanese Patent Application Serial No. 2000-544004, August 20, 2002, 4 pages (Japanese translation attached). Notification of Transmittal of the International Preliminary Examination Report for International Application C155 No. PCT/US99/07849, July 7, 2000, 7 pages. C156 Report of Reconsideration for Japanese Patent Application Serial No. 2000-544004. February 22, 2005, 6 pages (Japanese translation attached). C157 Written Opinion for International Application No. PCT/US99/07849, January 13, 2000, 6 pages. C158 Written Opinion for International Application No. PCT/US01/46322, January 22, 2003, 2 pages.

EXAMINER Qualter V. Owen	DATE CONSIDERED 10/05/05